

REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 6-7 and 15-20 have been cancelled without prejudice. Claims 1 and 8 have been amended. No claims are added or withdrawn. No new matter has been added.

Response to Rejections under 35 U.S.C. § 102(b)

The Office Action rejected claims 1-4, 6 and 7 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,834,014 (*Yoo*). Claims 6-7 have been cancelled without prejudice and, thus, the rejection of claims 6-7 is moot. The Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

Amended claim 1 recites:

A dynamic random access memory device, comprising:
an address bus interface;
an address bus termination circuit that can be enabled or disabled; ~~and~~
an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is tied to a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is tied to a second voltage level;
a data bus interface;
a data bus termination circuit that can be enabled or disabled; and .
a data bus termination control signal input, wherein the data bus termination control signal input is operable to enable the data bus termination circuit when the data bus termination control signal input is tied to a first voltage level, and wherein the data bus termination control signal input is operable to disable the data bus termination circuit when the data bus termination control signal input is tied to a second voltage level.

The Applicant respectfully submits that *Yoo* does not disclose a dynamic random access memory device having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input. Instead, *Yoo* merely discloses a memory device with a single termination circuit (see, e.g., RT42, shown in FIG. 4) which has an **internally** generated control signal (e.g., a control signal generated by active termination control signal generator 435, shown in FIG. 4). For at least the reason that *Yoo* does not disclose a memory device having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input *Yoo* cannot anticipate claim 1. Thus, the Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claims 2-4 depend from claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claims 2-4 are not anticipated by *Yoo*.

Claims 1-3 and 5-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,313,595 (*Lewis*). Claims 6-7 have been cancelled without prejudice and, thus, the rejection of claims 6-7 is moot. The Applicant respectfully submits that claims 1-3 and 5 are patentable over the cited reference because *Lewis* does not disclose all of the limitations of the claim.

The Applicant respectfully submits that *Lewis* does not disclose a dynamic random access memory device as recited in claim 1. Instead, *Lewis* merely discloses a termination scheme for a SCSI bus (see, e.g., the Abstract). For at least the reason that *Lewis* does not disclose a dynamic random access memory *Lewis* cannot anticipate claim 1. Thus, the Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claims 2-3 and 5 depend from claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claims 2-3 and 5 are not anticipated by *Lewis*.

Claims 8-10 and 13-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lewis (*Lewis*). Claims 15-18 have been cancelled without prejudice and, thus, the rejection of claims 15-18 is moot. The Applicant respectfully submits that claims 8-10 and 13-14 are patentable over the cited reference because *Lewis* does not disclose all of the limitations of the claim.

Amended claim 8 recites, in part, “a plurality of dynamic random access memory devices.” As shown above, *Lewis* does not disclose a dynamic random access memory device. Instead, *Lewis* merely discloses a termination scheme for a SCSI bus (see, e.g., the Abstract). For at least the reason that *Lewis* does not disclose a dynamic random access memory *Lewis* cannot anticipate claim 8. Thus, the Applicant respectfully requests that the rejection of claim 1 be withdrawn.

Claims 9-10 and 13-14 depend from claim 8. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claims 9-10 and 13-14 are not anticipated by *Lewis*.

Response to Rejections under 35 U.S.C. § 103(a)

The Manual of Patent Examining Procedure (“MPEP”), in § 706.02(j), states:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, **the prior art reference** (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the prior art and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(Emphasis added). Thus, the MPEP and applicable case law require that the Office action establish that a combination of references teach or suggest **all of the claim limitations** of rejected claims to sustain an obviousness rejection under 35 U.S.C. § 103. As shown

below, Applicants respectfully submit that the Office action does not establish a *prima facie* case of obviousness.

Claim 4 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Lewis* in view of *Janzen*. The Applicant respectfully submits that claim 4 is patentable over *Lewis* and *Janzen* for at least the reasons set forth below.

Claim 4 depends from claim 1, either directly or indirectly, and includes the limitations of claim 1. As shown above, claim 1 recites a dynamic random access memory device having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input. Neither *Lewis* nor *Janzen* teach or suggest the above referenced limitations and, thus, no combination of *Lewis* with *Janzen* can teach or suggest the referenced limitations. In particular, *Lewis* merely discloses a termination scheme for a SCSI bus (see, e.g., the Abstract). *Janzen* actually teaches away from claim 1 because it is directed to “a single active termination control line per memory module” (see, e.g., the Abstract). For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claim 4 is patentable over *Lewis* and *Janzen*.

Claim 5 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Yoo* in view of *Janzen*. The Applicant respectfully submits that claim 5 is patentable over *Yoo* and *Janzen* for at least the reasons set forth below.

Janzen is cited as teaching reverse logic states. Whether or not *Janzen* discloses the limitations cited by the Office action, it does not teach or suggest a dynamic random access memory device having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input, as recited in claim 1. Because neither *Yoo* nor *Janzen* teach or suggest the above-cited claim limitations, no combination of *Yoo* and *Janzen* teaches or suggests the invention as recited in claim 1. Claim 5 depends, either directly or indirectly, from claim 1. For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claim 5 is patentable over *Yoo* and *Janzen*.

Claim 11 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Lewis* in view of *Janzen*. The Applicant respectfully submits that claim 11 is patentable over *Lewis* and *Janzen* for at least the reasons set forth below.

Claim 11 depends from claim 8, either directly or indirectly, and includes the limitations of claim 8. Claim 8 recites a plurality dynamic random access memory devices each having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input. Neither *Lewis* nor *Janzen* teach or suggest the above referenced limitations and, thus, no combination of *Lewis* with *Janzen* can teach or suggest the referenced limitations. In particular, *Lewis* merely discloses a termination scheme for a SCSI bus (see, e.g., the Abstract). *Janzen* actually teaches away from claim 8 because it is directed to “a single active termination control line per memory module” (see, e.g., the Abstract). For at least the reason that dependent claims include the limitations of the claims from which they depend, the Applicant respectfully submits that claim 11 is patentable over *Lewis* and *Janzen*.

Claim 12 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Lewis* in view of *Janzen*. The Applicant respectfully submits that claim 12 is patentable over *Lewis* and *Janzen* for at least the reasons set forth below.

Claim 12 depends from claim 8, either directly or indirectly, and includes the limitations of claim 8. Claim 8 recites a plurality dynamic random access memory devices each having both an address bus termination circuit with an associated address bus termination control signal input **and** a data bus termination circuit with an associated data bus termination control signal input. Neither *Lewis* nor *Janzen* teach or suggest the above referenced limitations and, thus, no combination of *Lewis* with *Janzen* can teach or suggest the referenced limitations. In particular, *Lewis* merely discloses a termination scheme for a SCSI bus (see, e.g., the Abstract). *Janzen* actually teaches away from claim 8 because it is directed to “a single active termination control line per memory module” (see, e.g., the Abstract). For at least the reason that dependent claims include the

limitations of the claims from which they depend, the Applicant respectfully submits that claim 12 is patentable over *Lewis* and *Janzen*.

Claim 19 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Lewis* in view of *Janzen*. Claim 19 has been cancelled without prejudice and, thus, the rejection of claim 19 is moot.

Claim 20 was rejected under 35 U.S.C. § 103(a) as not being patentable over *Lewis* in view of *Janzen*. Claim 20 has been cancelled without prejudice and, thus, the rejection of claim 19 is moot.

CONCLUSION

Conclusion

The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Respectfully submitted,

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